

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet	1	of	1
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Complete if Known

Application Number	09/540,611
Filing Date	March 31, 2000
First Named Inventor	Carl M. Ellison
Art Unit	2134
Examiner Name	Ellen C. Tran
Attorney Docket Number	42390P8112

U.S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]

**Examiner
Signature**

Date	
Considered	

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Signature

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

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Based on PTO/SB/08A (08-03) as modified by Blakely, Sotokoff, Taylor & Zafman (wtr) 08/11/2003.

Send To: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

09/540,611

ECT

Reference No.	Application Serial No.	Patent No.	Title
1	09/672,603		Controlling Accesses To Isolated Memory Using A Memory Controller For Isolated Execution
2	09/822,986		Checking File Integrity Using Signature Generated In Isolated Execution
3	09/538,951		Platform And Method For Issuing And Certifying A Hardware-Protected Attestation Key
4	09/539,344		Managing A Secure Platform Using A Hierarchical Executive Architecture In Isolated Execution Mode
5	09/668,585		Managing A Secure Platform Using A Hierarchical Executive Architecture In Isolated Execution Mode
6	09/541,108		Platform And Method For Remote Attestation Of A Platform
7	09/540,612		Platform And Method For Generating And Utilizing A Protected Audit Log
8	09/540,946		Protecting Software Environment In Isolated Execution
9	09/668,610		Protecting Software Environment In Isolated Execution
10	09/538,954		Generating Isolated Bus Cycles For Isolated Execution
11	09/539,348	6,760,441	Generating A Key Hierarchy For Use In An Isolated Execution Environment
12	09/541,477	6,507,904	Isolated Instructions For Isolated Execution
13	09/540,611		Managing Accesses In A Processor For Isolated Execution
14	09/540,613		Managing A Secure Environment Using A Chipset In Isolated Execution Mode
15	09/668,408		Managing A Secure Environment Using A Chipset In Isolated Execution Mode
16	09/541,667		Attestation Key Memory Device And Bus
17	09/672,602		Attestation Key Memory Device And Bus
18	09/618,738	6,678,825	Controlling Access To Multiple Isolated Memories In An Isolated Execution Environment
19	09/618,489	6,633,963	Controlling Access To Multiple Memory Zones In An Isolated Execution Environment
20	10/683,542		Controlling Access To Multiple Memory Zones In An Isolated Execution Environment
21	09/618,659		Resetting A Processor In An Isolated Execution Environment
22	09/751,586		Resetting A Processor In An Isolated Execution Environment

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